|  |  |
| --- | --- |
| Id |  |
| Question | A microprocessor incorporates the functions of a computer's \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ |
| A | Central processing unit |
| B | Control processing unit |
| C | Central progressive unit |
| D | Arithmetic Logic Unit |
| Answer | A |
| Marks | 1 |
| Unit | 2 |

|  |  |  |
| --- | --- | --- |
| Id | |  |
| Question | | A \_\_\_\_\_\_\_\_\_\_\_\_program manages various routines aspects of the computer system on behalf of users and it is typically part of computer’s operating system. |
| A | | Input |
| B | | Supervisor |
| C | | User |
| D | | Output |
| Answer | | B |
| Marks | | 1 |
| Unit | | 2 |
| Id |  | |
| Question | In the event of an interrupt, the CPU \_\_\_\_\_\_\_\_\_\_\_ execution of the program that it is currently executing and transfers to an appropriate interrupt service subroutine. | |
| A | Stops | |
| B | Resumes | |
| C | Suspends | |
| D | Forces | |
| Answer | C | |
| Marks | 1 | |
| Unit | 2 | |

|  |  |
| --- | --- |
| Id |  |
| Question | A sequence of operations performed by the CPU in processing an instruction constitutes \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ |
| A | Input cycle |
| B | Output cycle |
| C | Instruction cycle |
| D | Clock Cycle |
| Answer | C |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | A time required for the shortest well defined CPU micro-operation is the \_\_\_\_\_\_\_\_\_\_\_\_ |
| A | Input cycle time |
| B | CPU cycle time |
| C | Instruction cycle time |
| D | memory cycle time |
| Answer | B |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | Interrupts which are initiated by an I/O drive are |
| A | Internal |
| B | External |
| C | Software |
| D | None of these |
| Answer | B |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | A Information can be transferred only in between two units at a time only in case of \_\_\_\_\_\_\_\_\_ |
| A | System bus organization |
| B | Single bus organization |
| C | Peripheral connection wires |
| D | Two bus organization |
| Answer | B |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | A pipeline is like |
| A | an automobile assembly line |
| B | a gas line |
| C | house pipeline |
| D | None of above |
| Answer | A |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | The I/O processor has a direct access to ....................... and contains a number of independent data channels. |
| A | secondary memory |
| B | main memory |
| C | cache memory |
| D | Flash memory |
| Answer | B |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | Pipelining increases the CPU instruction .......... |
| A | throughput |
| B | efficiency |
| C | latency |
| D | Both B and C |
| Answer | A |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | The I/O devices are associated with addressable registers called \_\_\_\_\_\_\_\_\_\_to which the CPU can store a word or from which CPU can load a word. |
| A | Data registers |
| B | Program counter |
| C | I/O ports |
| D | Instruction register |
| Answer | C |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | All I/O data transfers are implemented memory referencing instructions by an approach known as \_\_\_\_\_\_\_\_\_\_\_\_ |
| A | IO mapped IO |
| B | Memory mapped IO |
| C | IO operation |
| D | Memory operation |
| Answer | B |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | Some computers employ I/O instructions that produce control signals to which IO ports responds known as \_\_\_\_\_\_\_\_\_\_\_\_ |
| A | IO mapped IO |
| B | Memory mapped IO |
| C | IO operation |
| D | Memory operation |
| Answer | A |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | CPU speed is significantly faster than memory . To remedy this situation \_\_\_\_\_\_\_\_\_\_is introduced between CPU and main memory. |
| A | Secondary memory |
| B | External memory |
| C | Cache memory |
| D | Internal memory |
| Answer | C |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | A\_\_\_\_\_\_\_\_\_ program handles a specific application, such as word processing. |
| A | Supervisor |
| B | User |
| C | Input |
| D | Output |
| Answer | B |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | GS in 80386 DX architecture refers to \_\_\_\_\_\_\_\_ |
| A | Data segment register |
| B | Data register |
| C | Extra segment register |
| D | Both A & B |
| Answer | A |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | A CPU register called \_\_\_\_\_\_\_\_\_\_automatically keeps track of the next instruction that is to be executed. |
| A | Program counter |
| B | Accumulator |
| C | Memory register |
| D | A stack pointer |
| Answer | A |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | In accumulator based CPU which supports single address instructions, \_\_\_\_\_\_\_\_\_\_serves as implicit operand locations |
| A | Program counter |
| B | Address register |
| C | Data register |
| D | accumulator |
| Answer | D |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | Motorola 680X0 uses \_\_\_\_architecture. |
| A | RISC |
| B | CISC |
| C | RISC & CISC |
| D | None of these |
| Answer | A |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | Power-Pc microprocessor uses\_\_\_\_\_\_\_\_architecture. |
| A | RISC |
| B | CISC |
| C | RISC & CISC |
| D | None of these |
| Answer | A |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | A typical \_\_\_\_\_\_\_\_employes instructions of fixed length. |
| A | RISC |
| B | CISC |
| C | RISC & CISC |
| D | None of these |
| Answer | A |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | In \_\_\_\_\_\_\_\_\_memory addressing is restricted to load & store. |
| A | RISC |
| B | CISC |
| C | RISC & CISC |
| D | None of these |
| Answer | A |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | CISC stands for ................ |
| A | Complex Instruction Set Computers |
| B | Common Instruction Set Computers |
| C | Complex Instruction Set Compilers |
| D | Compound Instruction Set Computers |
| Answer | A |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | Memory access in RISC architecture is limited to instructions |
| A | CALL and RET |
| B | PUSH and POP |
| C | STA and LDA |
| D | MOV and JMP |
| Answer | C |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | Which is true for a typical RISC architecture? |
| A | Micro programmed control unit. |
| B | Instruction takes multiple clock cycles. |
| C | Have few registers in CPU. |
| D | Emphasis on optimizing instruction pipelines. |
| Answer | A |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | Which of the following is not a characteristic of a RISC architecture. |
| A | Large instruction set |
| B | One instruction per cycle |
| C | Simple addressing modes |
| D | Register-to-register operation |
| Answer | A |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | The overlapping of instruction fetching and execution i.e. instruction pipelining is important speed up feature of \_\_\_\_\_\_\_\_\_\_processor. |
| A | RISC |
| B | CISC |
| C | RISC & CISC |
| D | None of these |
| Answer | A |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | The Motorola 680X0 family is example of \_\_\_\_\_\_\_\_architecture. |
| A | RISC |
| B | CISC |
| C | RISC & CISC |
| D | None of these |
| Answer | B |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | The ARM6 microprocessor is example of \_\_\_\_\_\_\_\_architecture. |
| A | RISC |
| B | CISC |
| C | RISC & CISC |
| D | None of these |
| Answer | A |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | In RISC machine, set of general purpose registers is known as \_\_\_\_\_\_\_\_\_ |
| A | Register array |
| B | Register file |
| C | General purpose register |
| D | Register unit |
| Answer | B |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | In virtual mode, the paging unit allows only \_\_\_\_\_ pages |
| A | 32 |
| B | 64 |
| C | 256 |
| D | 128 |
| Answer | C |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | RISC memory operations are based on\_\_\_\_\_\_\_\_ |
| A | Address conversion technique |
| B | Load and store routine |
| C | Both A and B |
| D | Advanced Prefetching technique |
| Answer | B |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | Which of the following statements is false about RISC processor? |
| A | Fixed instruction size |
| B | Less instruction |
| C | Pipelining is used |
| D | Less number of registers |
| Answer | D |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | A\_\_\_\_\_\_\_\_\_\_ pipeline can double the CPU's performance from one instruction every two clock cycle to one instruction every clock cycle. |
| A | non |
| B | One stage |
| C | two stage |
| D | None of above |
| Answer | C |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | The\_\_\_\_\_\_\_\_\_\_\_ reduces the efficiency of instruction pipelining. |
| A | ADD instruction |
| B | Branch instruction |
| C | SUB instruction |
| D | Mul instruction |
| Answer | B |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | What is true about CISC? |
| A | Large number of addressing modes |
| B | Uses simple Instruction pipeline |
| C | Hardwired control unit |
| D | Limited & simple instruction set |
| Answer | A |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | RISC stands for |
| A | Resource Instruction Set Computer |
| B | Reduced Instruction Set Computer |
| C | Reduced Integrated Set Computer |
| D | Resource Instruction System Computer |
| Answer | B |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | CISC CPU has \_\_\_\_\_\_\_\_\_\_\_\_\_\_ control unit. |
| A | Hardwired |
| B | Microprogrammed |
| C | Both |
| D | None of these |
| Answer | B |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | Addressing modes in CISC ranges from ? |
| A | 12-24 |
| B | 9-12 |
| C | 3-5 |
| D | None of these |
| Answer | A |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | Addressing modes in RISC ranges from ? |
| A | 12-24 |
| B | 9-12 |
| C | 3-5 |
| D | None of these |
| Answer | C |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | The advantage of RISC processor over CISC processor is that |
| A | The hardware architecture is simpler |
| B | An instruction can be executed in one cycle |
| C | Less number of registers accommodate in chip |
| D | Parallel execution capabilities |
| Answer | B |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | Intel Pentium CPU is a |
| A | RISC based |
| B | CISC based |
| C | Both of the above |
| D | None of the above |
| Answer | C |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | The important feature of speedup of RISC processor is … |
| A | Instruction Pipelining |
| B | Instruction Cycle |
| C | Instruction Cycle time |
| D | Instruction Fetch time |
| Answer | A |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | Fast, single cycle instruction execution is harder to achieve with a …. |
| A | complex instruction set |
| B | Reduced instruction set |
| C | Instruction set |
| D | Instruction set computer |
| Answer | A |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | A set of general multipurpose registers in RISC machines is referred as\_\_\_\_\_. |
| A | Register array |
| B | Register file |
| C | Register unit |
| D | none of above |
| Answer | B |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | To indicate exceptional conditions resulting from instruction execution \_\_\_\_\_\_is used in RISC or CISC machines. |
| A | status register |
| B | program counter register |
| C | data register |
| D | address register |
| Answer | A |
| Marks | 1 |
| Unit | 2 |
| Id |  |
| Question | which of the following statement(s) is/are true about RISC processors |
| A | Instruction size is fixed |
| B | Number of instruction are less |
| C | Complex addressing modes are synthesized in software. |
| D | All of these |
| Answer | D |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | which of the following statement(s)is/are true about CISC processors? |
| A | Instruction size varies |
| B | number of instruction are more. |
| C | Supports complex addressing modes |
| D | All of these |
| Answer | D |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | which of the following statements is false about CISC processors ? |
| A | Instruction size varies. |
| B | Easy quick to decode |
| C | Supports complex addressing modes |
| D | Number of instruction are more |
| Answer | B |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | Which of the following statements is false about RISC processors ? |
| A | Instruction size is fixed. |
| B | Number of instruction are less |
| C | Complex addressing modes are synthesized in software. |
| D | Less number of registers |
| Answer | D |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | The ARM6 employs an instruction Pipeline to meet the goal of \_\_\_\_\_\_instruction executed per CPU clock cycle. |
| A | Multiple |
| B | One |
| C | Two |
| D | None of above |
| Answer | B |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | In 680X0 family of CISC machines register file contain \_\_\_\_\_\_\_ general purpose registers. |
| A | 8 |
| B | 32 |
| C | 16 |
| D | None of above |
| Answer | C |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | The 80386 can run 8086 applications under\_\_\_\_\_\_\_\_. |
| A | Promiscuous mode |
| B | Real mode |
| C | Protected mode |
| D | Logical mode |
| Answer | C |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | Auxiliary microprocessor is coupled with main microprocessor to carry out complex numerical calculations is called as |
| A | Micro controller |
| B | Coprocessor |
| C | Dual processor |
| D | Ad-on processor |
| Answer | B |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | When coprocessor executes its own instruction, main processor \_\_\_\_. |
| A | waits until co-processor's execution completed |
| B | stops executing any further instruction |
| C | executes its own instructions simultaneously |
| D | none of above |
| Answer | C |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | Which of the following statement(s)is/are true about coprocessors ? |
| A | Coprocessor has its own instruction set. |
| B | CPU and coprocessor execute their instructions from the same program |
| C | CPU and coprocessor share entire memory and the I/O subsystem |
| D | All of these. |
| Answer | D |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | The advantage of RISC processor over CISC processor is that |
| A | The hardware architecture is simpler |
| B | An instruction can be executed in one cycle |
| C | Less number of registers accommodate in chip |
| D | Parallel execution capabilities |
| Answer | B |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | Intel Pentium CPU is a |
| A | RISC based |
| B | CISC based |
| C | Both of the above |
| D | None of the above |
| Answer | A |
| Marks | 1 |
| Uni t | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | Instruction format for RISC is |
| A | 32 bit fixed |
| B | 64 bit fixed |
| C | 16 bit fixed |
| D | 64 bit variable |
| Answer | A |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | CISC has \_\_\_\_\_\_\_\_\_\_\_\_\_\_ control unit |
| A | Hardwired |
| B | Microprogrammed |
| C | Both |
| D | None of these |
| Answer | B |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | Addressing modes in CISC ranges from ? |
| A | 12-24 |
| B | 9-12 |
| C | 3-5 |
| D | 25-50 |
| Answer | A |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | Addressing modes in RISC ranges from ? |
| A | 12-24 |
| B | 9-12 |
| C | 3-5 |
| D | 25-50 |
| Answer | C |
| Marks | 1 |
| Unit | 2 |

|  |  |  |
| --- | --- | --- |
| Id |  | |
| Question | Memory mapped I/O approach requires that memory locations and I/O ports share \_\_\_\_ set of addresses. | |
| A | Same | |
| B | Different | |
| C | May same | |
| D | All of the above | |
| Answer | A | |
| Marks | 1 | |
| Unit | 2 | |
| Id | |  |
| Question | | Controlling a graphics interface is the function of ? |
| A | | User program |
| B | | Application program |
| C | | Supervisor program |
| D | | Interrupt program |
| Answer | | C |
| Marks | | 1 |
| Unit | | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | The CPU operation is specified by a binary code known as\_\_\_\_\_\_\_. |
| A | Operand code |
| B | Source code |
| C | Bytecode |
| D | Opcode |
| Answer | D |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | IPS is\_\_\_\_\_\_\_\_\_\_. |
| A | Instructions executed per second |
| B | Instructions executed per cycle |
| C | Instructions executed per system |
| D | Instructions executed per set |
| Answer | A |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | The data on which the operation is to be performed is indicated as \_\_\_\_\_\_\_\_\_\_ . |
| A | Operand |
| B | Instruction |
| C | Opcode |
| D | Program |
| Answer | A |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | \_\_\_\_\_\_ are used to overcome the difference in data transfer speeds of various devices. |
| A | Speed enhancing circuitry |
| B | Bridge circuits |
| C | Multiple Buses |
| D | Buffer registers |
| Answer | D |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | To extend the connectivity of the processor bus we use \_\_\_\_\_\_ . |
| A | PCI bus |
| B | SCSI bus |
| C | Controllers |
| D | Multiple bus |
| Answer | A |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | In multiple Bus organization, the registers are collectively placed and referred as \_\_\_\_\_\_ . |
| A | Set registers |
| B | Register file |
| C | Register Block |
| D | Map registers |
| Answer | B |
| Marks | 1 |
| Unit | 2 |

|  |  |  |
| --- | --- | --- |
| Id |  | |
| Question | The main advantage of multiple bus organization over single bus is | |
| A | Reduction in the number of cycles for execution | |
| B | Increase in size of the registers | |
| C | Better Connectivity | |
| D | None of these | |
| Answer | A | |
| Marks | 1 | |
| Unit | 2 | |
| Id | |  |
| Question | | \_\_\_\_\_\_ addressing operand is actually present in the instruction. |
| A | | Immediate |
| B | | Direct |
| C | | Register |
| D | | None of the above |
| Answer | | A |
| Marks | | 1 |
| Unit | | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | Primary Function of CPU is |
| A | To execute sequence of instructions |
| B | Only to bring the instructions into main memory |
| C | Decide the sequence of micro operations |
| D | None of these |
| Answer | A |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | Cache Memory is ---------than main memory. |
| A | Cheaper |
| B | smaller and faster |
| C | Slower and bigger |
| D | Costlier |
| Answer | B |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | A supervisor program is used to manage … |
| A | Various routine aspects of the computer system on behalf of its user. |
| B | Manage user program |
| C | Request for supervisor services. |
| D | Temporarily suspended execution |
| Answer | A |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | Sequence of micro operations are used to determine …. |
| A | The actions of the CPU |
| B | Basic task of CPU |
| C | Opcode of Instruction |
| D | Operand |
| Answer | A |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | \_\_\_\_\_Program is a part of computer operating system. |
| A | Application |
| B | User |
| C | Supervisory |
| D | None of above |
| Answer | C |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | When I/O data transfers are implemented by memory referencing instruction, it is referred as\_\_\_\_\_\_\_\_ |
| A | memory mapped I/O |
| B | memory mapped memory |
| C | I/O mapped memory |
| D | I/O mapped IO |
| Answer | A |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | Register which is used as source register for ALU and also used to store result of operation performed in ALU is called\_\_\_\_\_\_ |
| A | Source register |
| B | data register |
| C | Dual register |
| D | Accumulator |
| Answer | D |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | Which of the following is/are the components of Data Processing Unit (DPU) ? |
| A | n-bit Arithmetic Logic Unit (ALU) |
| B | AC |
| C | DR |
| D | All of these |
| Answer | D |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | ‘Load’ instruction belongs to \_\_\_\_\_\_\_group of instructions. |
| A | Data transfer |
| B | Data processing |
| C | Program control |
| D | None of these |
| Answer | A |
| Marks | 1 |
| Unit | 2 |
| Id |  |
| Question | ‘Not’ instruction belongs to \_\_\_\_\_\_\_group of instructions. |
| A | Data transfer |
| B | Data processing |
| C | Program control |
| D | None of these |
| Answer | B |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | ‘Branch’ instruction belongs to \_\_\_\_\_\_\_group of instructions. |
| A | Data transfer |
| B | Data processing |
| C | Program control |
| D | None of these |
| Answer | C |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | A \_\_\_\_\_\_\_\_\_\_ is used to indicate computation status or exceptional conditions resulting from execution of instruction. |
| A | Status register |
| B | Data register |
| C | Program counter |
| D | None of these |
| Answer | A |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | \_\_\_\_keeps track of address location in stack memory |
| A | Address register |
| B | Stack pointer |
| C | Program counter |
| D | None of above |
| Answer | B |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | The overlapping of instruction fetching and instruction execution is an example of \_\_\_\_ |
| A | instruction sharing |
| B | instruction multiplexing |
| C | instruction pipelining |
| D | none of above |
| Answer | C |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | \_\_\_\_\_ instructions reduces the efficiency of the instruction pipelining. |
| A | Branch |
| B | Data transfer |
| C | Arithmetic |
| D | All the above |
| Answer | A |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | Memory mapped IO approach requires memory locations and IO ports share \_\_\_\_ set of addresses. |
| A | Same |
| B | Different |
| C | May same |
| D | All of the above |
| Answer | A |
| Marks | 1 |
| Unit | 2 |
| Id |  |
| Question | Controlling a graphics interface is the function of ?? |
| A | User program |
| B | Application program |
| C | Supervisor program |
| D | Interrupt program |
| Answer | C |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | \_\_\_\_\_is a basic unit of time for measuring CPU actions. |
| A | CPU cycle beat |
| B | CPU cycle tick |
| C | CPU cycle clock |
| D | CPU cycle time |
| Answer | D |
| Marks | 1 |
| Unit | 2 |
| Id |  |
| Question | IPS is\_\_\_\_\_\_\_\_\_\_?? |
| A | Instructions executed per second |
| B | Instructions executed per cycle |
| C | Instructions executed per system |
| D | Instructions executed per set |
| Answer | A |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | The code that indicates the operation to be performed is called as\_\_\_\_\_\_\_\_\_\_ |
| A | Operand |
| B | Instruction |
| C | Opcode |
| D | Program |
| Answer | C |
| Marks | 1 |
| Unit | 2 |
| Id |  |
| Question | \_\_\_\_\_\_ are used to overcome the difference in data transfer speeds of various devices . |
| A | Speed enhancing circuitry |
| B | Bridge circuits |
| C | Multiple Buses |
| D | Buffer registers |
| Answer | D |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | To extend the connectivity of the processor bus we use \_\_\_\_\_\_ |
| A | PCI bus |
| B | SCSI bus |
| C | Controllers |
| D | Multiple bus |
| Answer | A |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | In multiple Bus organization, the registers are collectively placed and referred as \_\_\_\_\_\_ . |
| A | Set registers |
| B | Register file |
| C | Register Block |
| D | Map registers |
| Answer | B |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | The main advantage of multiple bus organization over single bus is, |
| A | Reduction in the number of cycles for execution |
| B | Increase in size of the registers |
| C | Better Connectivity |
| D | None of these |
| Answer | A |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | The registers, ALU and the interconnecting path together are called as \_\_\_\_\_\_. |
| A | Control path |
| B | Flow path |
| C | Data path |
| D | None of the above |
| Answer | C |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | A \_\_\_\_\_\_\_\_\_\_ is a computer processor used to supplement the functions of \_\_\_\_\_\_\_\_. |
| A | microprocessor ,CPU |
| B | coprocessor ,CPU |
| C | micro controller ,microprocessor |
| D | ALU, CPU |
| Answer | B |
| Marks | 2 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | Negative numbers cannot be represented in \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ |
| A | Signed magnitude form |
| B | 1's complement form |
| C | 2's complement form |
| D | None of these |
| Answer | D |
| Marks | 2 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | The coprocessor serves as and extension to the\_\_\_\_\_\_\_\_\_ and forms a part of the \_\_\_\_\_\_\_. |
| A | CPU, Microprocessor |
| B | Micro controller , CPU |
| C | CPU , ALU |
| D | Microprocessor ,CPU |
| Answer | D |
| Marks | 2 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | The two main number formats are \_\_\_\_\_\_\_\_\_and \_\_\_\_\_\_\_\_\_\_\_\_. |
| A | Numerical, non-numerical |
| B | Fixed point , floating point |
| C | Fixed point , data |
| D | Numerical, floating point |
| Answer | B |
| Marks | 2 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | A fixed point format is derived directly from the ordinary representation of a number as a sequence of \_\_\_\_\_\_\_\_\_separated by a \_\_\_\_\_\_\_\_\_\_\_. |
| A | Numbers , floating point |
| B | Digits , decimal point |
| C | Numbers , decimal point |
| D | Digits , floating point |
| Answer | B |
| Marks | 2 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | Three numbers are associated with a floating point number : \_\_\_\_\_\_\_\_\_\_\_\_\_\_, \_\_\_\_\_\_\_\_\_\_\_\_\_\_,and \_\_\_\_\_\_\_\_\_\_\_. |
| A | Base , fixed point number, hex number |
| B | Mantissa , exponent, base |
| C | Weighted number, non weighted number, base |
| D | None of these |
| Answer | B |
| Marks | 2 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | The mantissa is said to be\_\_\_\_\_\_\_\_\_\_\_\_ if the digit to the right of the radix point is not zero. e.g. 0.1\*1019 is the unique \_\_\_\_\_\_\_\_\_\_ form of quintillion. |
| A | Normalized , exponent |
| B | Normalized , normal |
| C | Unique , exponent |
| D | Unique , normalized |
| Answer | B |
| Marks | 2 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | The smallest non zero positive number in floating point representation is \_\_\_\_\_\_\_\_\_\_\_\_;\_\_\_\_\_\_\_\_\_\_\_\_\_. |
| A | (001,111) , (101,111) |
| B | (001,111) , (111,111) |
| C | (111,111) , (101,111) |
| D | (011,111) , (100,111) |
| Answer | A |
| Marks | 2 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | The largest representable positive number in floating point representation is \_\_\_\_\_\_\_\_\_\_\_\_;\_\_\_\_\_\_\_\_\_\_\_\_\_. |
| A | (001,111) , (101,111) |
| B | (001,111) , (111,111) |
| C | (111,111) , (101,111) |
| D | (011,011) , (111,011) |
| Answer | D |
| Marks | 2 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | For floating point processing circuits include a few extra mantissa digits termed\_\_\_\_\_\_\_\_\_\_ to reduce \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ errors. |
| A | Normalized digits, approximation |
| B | guard digits, approximation |
| C | Guard digits, normalization |
| D | Normalized digits,normalization |
| Answer | B |
| Marks | 2 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | The coprocessor uses \_\_\_\_\_\_\_ signal when it needs to read or write data from memory |
| A | Busy' |
| B | Busy' and ERROR' |
| C | ERROR' |
| D | PEREQ |
| Answer | D |
| Marks | 2 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | Which of the following is/are the status signals from the coprocessor? |
| A | Busy' |
| B | Busy' and ERROR' |
| C | ERROR' |
| D | PEREQ |
| Answer | B |
| Marks | 2 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | Which of the following is not the status signal from the coprocessor? |
| A | Busy' |
| B | Busy' and ERROR' |
| C | ERROR' |
| D | PEREQ |
| Answer | D |
| Marks | 2 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | BUSY, ERROR and PEREQ are \_\_\_\_\_\_interface signals. |
| A | Interpreter |
| B | DMA |
| C | Coprocessor |
| D | None of these |
| Answer | C |
| Marks | 2 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | Binary numbers can also be expressed in this same notation by \_\_\_\_\_\_\_\_\_representation: |
| A | Floating point |
| B | Binary point |
| C | Decimal point |
| D | All of these |
| Answer | A |
| Marks | 2 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | The 12 bit binary number has a accuracy equivalent to decimal fraction \_\_\_\_\_\_\_\_\_ |
| A | 1/1024 |
| B | 1/2048 |
| C | 1/4096 |
| D | 1/8192 |
| Answer | C |
| Marks | 2 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | The first or the integer part of a value representation is known as\_\_\_\_\_\_\_\_ |
| A | None of these |
| B | Binomial |
| C | Integer |
| D | Exponent |
| Answer | A |
| Marks | 2 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | Which number is said to be normalized if the more significant position of the mantissa contains a non zero digit |
| A | Binary point number |
| B | Mantissa point number |
| C | Floating point number |
| D | None of these |
| Answer | C |
| Marks | 2 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | Binary numbers can also be expressed in this same notation by \_\_\_\_\_\_\_\_\_representation. |
| A | Decimal point |
| B | Floating point |
| C | Binary point |
| D | All of these |
| Answer | B |
| Marks | 2 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | Which of the following bit patterns represents the value 5 in two’s complement notation? |
| A | 00011010 |
| B | 11111011 |
| C | 00000101 |
| D | 11111011 |
| Answer | C |
| Marks | 2 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | In which of the following addition problems (using two?s complement notation) does an overflow error occur? |
| A | 0011  + 1010 |
| B | 0100  + 0100 |
| C | 1100  +1100 |
| D | None of the above |
| Answer | B |
| Marks | 2 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | In immediate addressing the operand is placed after \_\_\_\_\_\_ in the\_\_\_\_\_\_\_\_\_\_\_\_\_\_. |
| A | Opcode , instruction register |
| B | operand , in the CPU |
| C | operand , instruction register |
| D | Opcode , in stack |
| Answer | A |
| Marks | 2 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | In immediate addressing the operand is placed in the \_\_\_\_\_\_\_\_\_ after \_\_\_\_\_\_\_\_. |
| A | CPU register , Opcode |
| B | instruction , Opcode |
| C | instruction ,operand |
| D | Stack , operand |
| Answer | A |
| Marks | 2 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | Extra logic circuits and processing time needed to computer addresses are main drawbacks of \_\_\_\_\_\_\_\_\_\_\_ addressing mode. |
| A | Absolute |
| B | Immediate |
| C | relative |
| D | Direct |
| Answer | C |
| Marks | 2 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | The addressing mode used in an instruction of form MOVE #99,D1 is \_\_\_\_\_\_\_\_\_\_\_\_ |
| A | Immediate & register Direct |
| B | Relative |
| C | Indirect |
| D | Immediate & register Indirect |
| Answer | A |
| Marks | 2 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | The addressing mode used in an instruction of form ADD X,Y is \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ |
| A | indirect |
| B | Absolute |
| C | Immediate |
| D | direct |
| Answer | D |
| Marks | 2 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | If the value V(X) of the target operand is contained in the address field itself in an instruction, then addressing mode of X is called \_\_\_\_\_\_\_\_\_\_ . |
| A | An index operand |
| B | an immediate addressing mode |
| C | an immediate operand |
| D | Relative operand |
| Answer | C |
| Marks | 2 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | 'MOVE.B(A0),D1' instruction uses \_\_\_\_\_\_\_\_\_\_addressing. |
| A | Register indirect |
| B | Register Direct |
| C | Absolute |
| D | Immediate |
| Answer | A |
| Marks | 2 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | 'SW Rt,OFFSET(Rs)' instruction uses \_\_\_\_\_\_\_\_\_\_addressing. |
| A | Register indirect with offset |
| B | Direct with offset |
| C | Absolute with offset |
| D | Immediate with offset |
| Answer | A |
| Marks | 2 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | 'MOVE #99,D1' means \_\_\_\_\_\_\_\_\_\_\_\_\_ |
| A | load the constant 99 from data register D1. |
| B | store data register D1 with the value from location #99. |
| C | move the constant 99 to data register D1. |
| D | None of these |
| Answer | C |
| Marks | 2 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | 'LOADI 999' instruction uses \_\_\_\_\_\_\_\_\_\_addressing. |
| A | Register indirect |
| B | Register Direct |
| C | Absolute |
| D | Immediate |
| Answer | D |
| Marks | 2 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | 'LOAD X' instruction uses \_\_\_\_\_\_\_\_\_\_addressing. |
| A | indirect |
| B | Direct |
| C | Absolute |
| D | Immediate |
| Answer | B |
| Marks | 2 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | 'LOADN W' instruction uses \_\_\_\_\_\_\_\_\_\_addressing. |
| A | indirect |
| B | Direct |
| C | Absolute |
| D | Immediate |
| Answer | A |
| Marks | 2 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | mov al, [ebx] is an example of \_\_\_\_\_\_\_\_\_\_\_\_\_addressing mode. |
| A | Register Indirect |
| B | Direct |
| C | Indexed |
| D | None of above |
| Answer | A |
| Marks | 2 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | For PUSH and POP instruction , which addressing mode used is \_\_\_\_\_\_\_\_\_ |
| A | Register addressing |
| B | auto index |
| C | Index addressing |
| D | Direct addressing |
| Answer | B |
| Marks | 2 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | The ability to use all addressing modes in a uniform and consistent way with all opcodes of an instruction set or assembly language is a desirable feature termed \_\_\_\_\_\_\_\_\_\_\_\_\_. Many \_\_\_\_\_\_\_\_\_computers have this feature. |
| A | Addressing ,CISC |
| B | addressing , RISC |
| C | Orthogonality , CISC |
| D | None of these |
| Answer | C |
| Marks | 2 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | mov al,8[ebx][esi\*4] semantics of the this instruction is \_\_\_\_\_\_\_\_\_ in case value of ebx is 1000h and esi is 4. |
| A | Loads AL from location 1028h |
| B | Loads AL from location 1008h |
| C | Loads AL from location 1016h |
| D | Loads AL from location 1018h |
| Answer | D |
| Marks | 2 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | In which addressing mode the address field references the main memory and the referenced register contains a positive displacement from that address? |
| A | Relative addressing |
| B | Displacement addressing |
| C | Index addressing |
| D | Base register addressing |
| Answer | C |
| Marks | 2 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | To which addressing mode the following instruction belongs? MOV (R2) +, R0 |
| A | Index addressing |
| B | Base register addressing |
| C | Relative addressing |
| D | Auto-increment addressing |
| Answer | D |
| Marks | 2 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | To which addressing mode the following instruction belongs?  JNZ GOTO |
| A | Base register addressing |
| B | Relative addressing |
| C | Index Addressing |
| D | Register indirect addressing |
| Answer | B |
| Marks | 2 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | To which addressing mode the following instruction belongs?  MOV B, [R + 5] |
| A | Relative addressing |
| B | Base register addressing |
| C | Index addressing |
| D | Displacement addressing |
| Answer | B |
| Marks | 2 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | In which addressing mode the contents of a register specified instruction are decremented and then used as an effective address to access a memory location? |
| A | Base register addressing |
| B | Auto increment addressing |
| C | Auto decrement addressing |
| D | Stack addressing |
| Answer | C |
| Marks | 2 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | To which addressing mode the following instruction belongs ?MOV R1, - (R0) |
| A | Base register addressing |
| B | Auto increment addressing |
| C | Auto decrement addressing |
| D | Stack addressing |
| Answer | C |
| Marks | 2 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | In stack addressing mode, stack pointer contains address of \_\_\_\_\_\_\_of stack. |
| A | Bottom |
| B | Top |
| C | Middle |
| D | None of these |
| Answer | B |
| Marks | 2 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | To which addressing mode following instruction belongs?PUSH R |
| A | Stack addressing mode |
| B | Displacement addressing mode |
| C | Relative addressing mode |
| D | Index addressing mode |
| Answer | A |
| Marks | 2 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | In which addressing, the effective address is computed by adding contents of referenced register to value? |
| A | Relative addressing |
| B | Index addressing |
| C | Displacement addressing |
| D | Indirect addressing |
| Answer | C |
| Marks | 2 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | The two address instruction ADD A, B stores the sum of both A and B in \_\_\_\_\_\_\_\_ |
| A | A |
| B | B |
| C | Accumulator |
| D | None of these |
| Answer | A |
| Marks | 2 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | Instruction formats contains the memory address of the\_\_\_\_\_\_ |
| A | CPU |
| B | ALU |
| C | Main memory |
| D | Main data |
| Answer | C |
| Marks | 2 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | Which register holds the item that is to be written into the stack or read out of the stack? |
| A | IR |
| B | MAR |
| C | MBR |
| D | DR |
| Answer | D |
| Marks | 2 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | In which mode the main memory location holds the effective address of the operand |
| A | Immediate addressing |
| B | Direct addressing |
| C | Register addressing |
| D | Indirect addressing |
| Answer | D |
| Marks | 2 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | The simplest addressing mode where an operand is fetched from memory is\_\_\_\_\_ |
| A | Immediate addressing |
| B | Direct addressing |
| C | Register addressing |
| D | Indirect addressing |
| Answer | B |
| Marks | 2 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | In which addressing the operand is actually present in instruction |
| A | Immediate addressing |
| B | Direct addressing |
| C | Register addressing |
| D | Indirect addressing |
| Answer | A |
| Marks | 2 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | The instruction set can have variable-length instruction format primarily due to: |
| A | Varying number of operands |
| B | Varying length of opcodes in some CPU |
| C | Both |
| D | None |
| Answer | C |
| Marks | 2 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | A small and fixed-size instruction set that contains only a limited number of op-codes, is the example of? |
| A | RISC |
| B | CISC |
| C | Both |
| D | None |
| Answer | A |
| Marks | 2 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | Zero address instruction format is used for |
| A | RISC architecture |
| B | CISC architecture |
| C | Von-Neuman architecture. |
| D | Stack-organized architecture |
| Answer | D |
| Marks | 2 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | The machine instructions are in the \_\_\_\_\_ form . |
| A | hexadecimal code |
| B | octal code |
| C | binary code |
| D | none of these |
| Answer | C |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | \_\_\_\_\_tells the CPU from where to fetch the next instruction after completion of execution of current instruction. |
| A | Source operand address |
| B | destination operand address |
| C | Next instruction address |
| D | None of these |
| Answer | C |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | The \_\_\_\_\_ instructions provide computational capabilities for processing numeric data. |
| A | Arithmetic |
| B | Logical |
| C | Memory |
| D | Data transfer |
| Answer | A |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | \_\_\_\_\_ instructions are used to test the value of a data word or status of a computation. |
| A | Branch |
| B | Test |
| C | Logic |
| D | None of these |
| Answer | B |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | In zero address instructions, the locations of all operands are defined \_\_\_\_\_. |
| A | Explicitly |
| B | Implicitly |
| C | Both a and b |
| D | None of these |
| Answer | B |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | The one address instruction ADD B adds the contents of variable B into processor register called as \_\_\_\_\_. |
| A | Stack |
| B | Accumulator |
| C | Both a and b |
| D | None of these |
| Answer | B |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | The \_\_\_\_\_\_\_ phase interprets the opcode by decoding it. |
| A | Decode |
| B | Fetch |
| C | Execute |
| D | None of these |
| Answer | A |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | The \_\_\_\_\_\_phase performs the desired operation in the instruction. |
| A | Decode |
| B | Fetch |
| C | Execute |
| D | None of these |
| Answer | C |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | An 8-bit register containing in the binary value 10011100 then what is the register value after arithmetic shift right? |
| A | 11001110 |
| B | 00111000 |
| C | 11000110 |
| D | None of these |
| Answer | A |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | An 8-bit register contains the binary value 10011100, then what are the contents of register after an arithmetic Shift left? |
| A | 11001110 |
| B | 00111000 |
| C | 11000110 |
| D | None of these |
| Answer | B |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | 1 Kbytes memory requires how many address bits? |
| A | 20 |
| B | 10 |
| C | 15 |
| D | 12 |
| Answer | B |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | 220= ------ |
| A | 2 kbytes |
| B | 100 kbytes |
| C | 1 mbytes |
| D | 2 mbytes |
| Answer | C |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | A smallest,closest and fastest internal memory is called ……, needed by the processor. |
| A | Registers |
| B | Shifters |
| C | Cache |
| D | None of these |
| Answer | A |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | More opcodes and more operands ……… program length to accomplish given task. |
| A | Reduce |
| B | Increases |
| C | Keep Constant |
| D | None of these |
| Answer | A |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | Due to variable length instructions, decoding of instruction becomes ……. |
| A | Easy |
| B | Difficult |
| C | Impossible |
| D | None of these |
| Answer | B |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | A processor can access data by different ways are referred as ……. |
| A | Addresses |
| B | Addressing modes |
| C | Operation Modes |
| D | Fetching |
| Answer | B |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | The instruction length should be equal to or multiple of ….. bus length |
| A | Data |
| B | Address |
| C | Control |
| D | System |
| Answer | A |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | The \_\_\_\_\_ phase interprets the opcode by decoding it. |
| A | Fetch |
| B | Decode |
| C | Execute |
| D | None of these |
| Answer | B |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | The unit which decodes and translates each instruction and generates the necessary enable signals for ALU and other units is called .. |
| A | arithmetic unit |
| B | Control Unit |
| C | logical unit |
| D | A and C |
| Answer | B |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | A list of instructions used by a computer is called |
| A | program |
| B | CPU |
| C | text |
| D | output |
| Answer | A |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | Which of the following are not a machine instructions |
| A | MOV |
| B | ORG |
| C | END |
| D | B & C |
| Answer | D |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | In Assembly language programming, minimum number of operands required for an instruction is/are |
| A | zero |
| B | one |
| C | two |
| D | Both B & C |
| Answer | A |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | The instructions which copy information from one location to another either in the processor’s internal register set or in the external main memory are called |
| A | Data transfer instructions |
| B | Program control instructions |
| C | Input-output instructions |
| D | Logical instructions |
| Answer | A |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | Which activity does not take place during execution cycle? |
| A | ALU performs the arithmetic & logical operation |
| B | Effective address is calculated |
| C | Next instruction is fetched |
| D | Branch address is calculated & Branching conditions are checked. |
| Answer | D |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | Pseudo instructions are |
| A | Machine instructions |
| B | Logical instructions |
| C | Micro instructions |
| D | instructions to assembler. |
| Answer | A |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | Computers use addressing mode techniques for \_\_\_\_ |
| A | giving programming versatility to the user by providing facilities as pointers to memory counters for loop control |
| B | to reduce no. of bits in the field of instruction |
| C | specifying rules for modifying or interpreting address field of the instruction |
| D | All the above |
| Answer | D |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | In a program using subroutine call instruction, it is necessary |
| A | Initialise program counter |
| B | Clear the accumulator |
| C | Reset the microprocessor |
| D | Clear the instruction register |
| Answer | D |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | A Stack-organised Computer uses instruction of |
| A | Indirect addressing |
| B | Two-addressing |
| C | Zero addressing |
| D | Index addressing |
| Answer | C |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | MIMD stands for |
| A | Multiple instruction multiple data |
| B | Multiple instruction memory data |
| C | Memory instruction multiple data |
| D | Multiple information memory data |
| Answer | A |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | The load instruction is mostly used to designate a transfer from memory to a processor register known as |
| A | Accumulator |
| B | Instruction Register |
| C | Program counter |
| D | Memory address Register |
| Answer | A |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | MRI indicates |
| A | Memory Reference Information. |
| B | Memory Reference Instruction. |
| C | Memory Registers Instruction. |
| D | Memory Register information |
| Answer | B |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | The instructions which copy information from one location to another either in the processor’s internal register set or in the external main memory are called |
| A | Data transfer instructions |
| B | Program control instructions |
| C | Input-output instructions |
| D | Logical instructions |
| Answer | A |
| Marks | 1 |
| Unit | 2 |

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|  |  |
| --- | --- |
| Id |  |
| Question | Which operation stops the program execution? |
| A | Halt |
| B | Wait |
| C | Skip |
| D | None of these |
| Answer | A |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | \_\_\_\_\_ Operation gives status information from I/O system to specified destination |
| A | Input |
| B | Start I/O |
| C | Test I/O |
| D | None of these |
| Answer | C |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | \_\_\_\_\_ Operation is used to transfer word from top of stack to destination. |
| A | Push |
| B | Move |
| C | Load |
| D | Pop |
| Answer | D |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | Which operation changes the sign of operand? |
| A | Absolute |
| B | Negate |
| C | Increment |
| D | None of these |
| Answer | B |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | Test I/O transfers status information from\_\_\_\_to\_\_\_\_. |
| A | I/O system, specified destination |
| B | specified destination I/O system |
| C | processor, I/O system |
| D | None of these |
| Answer | A |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | Convert operation converts the content of a word from\_\_\_\_\_\_\_\_\_ to\_\_\_\_\_\_\_\_\_\_\_\_\_. |
| A | Positive,Negative |
| B | Negative,Positive |
| C | one form, another |
| D | none of these |
| Answer | C |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | Test operation tests specified condition and sets \_\_\_\_\_\_\_\_\_\_\_ |
| A | Source |
| B | Destination |
| C | Flags |
| D | Accumulator |
| Answer | C |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | NOP operation means\_\_\_\_\_ . |
| A | Does not perform any operation. |
| B | stops program execution |
| C | Starts program execution |
| D | halts program execution |
| Answer | A |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | \_\_\_\_\_operation increments PC to next instruction |
| A | Execute |
| B | Skip |
| C | Delete |
| D | None of these |
| Answer | B |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | The character code IRA stand for |
| A | International Reference Alphabet |
| B | International Register Alphabet |
| C | International Research Alphabet |
| D | None of these |
| Answer | A |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | Halt operation \_\_\_\_ program execution. |
| A | Stop |
| B | Start |
| C | Temporally stop |
| D | None of these |
| Answer | A |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | ASCII Represents as |
| A | American Standard Code for Indian Information |
| B | American Standard Code for Information Interchange |
| C | American Standard Code for International Information |
| D | African Standard Code for Information Interchange |
| Answer | B |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | For Pentium ,which of the following are not referred as general data types. |
| A | Byte |
| B | Bit |
| C | Word |
| D | Double word |
| Answer | B |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | In three address instruction ADD A, B, C which of the following is true? |
| A | A and B are source operands and C is destination operands |
| B | A is source operand and B, C are destination operands |
| C | A, B, C are source operands |
| D | A, C are source operands and B is destination operands. |
| Answer | A |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | After performing Logical right shift(3 bits) of 10100110, the result is\_\_\_\_ |
| A | 00011100 |
| B | 00010100 |
| C | 00010110 |
| D | 00010010 |
| Answer | B |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | After performing Logical left shift(3 bits) of 10100110, the result is\_\_\_\_ |
| A | 00110100 |
| B | 00111000 |
| C | 00110000 |
| D | 00101000 |
| Answer | C |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | After performing Arithmetic right shift(3 bits) of 10100110, the result is\_\_\_\_ |
| A | 11110111 |
| B | 11110100 |
| C | 11110101 |
| D | 11110100 |
| Answer | D |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | After performing Arithmetic left shift(3 bits) of 10100110, the result is\_\_\_\_ |
| A | 10110000 |
| B | 10110001 |
| C | 10111000 |
| D | 10110010 |
| Answer | A |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | After performing right rotate (3 bits) of 10100110, the result is\_\_\_\_ |
| A | 11010101 |
| B | 11010100 |
| C | 11010110 |
| D | 11010000 |
| Answer | B |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | After performing left rotate(3 bits) of 10100110, the result is\_\_\_\_ |
| A | 00110010 |
| B | 00110101 |
| C | 00111100 |
| D | 00011100 |
| Answer | B |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | 80386 processor supports overall \_\_\_\_\_\_\_\_ types of addressing modes |
| A | 10 |
| B | 11 |
| C | 12 |
| D | 13 |
| Answer | B |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | In 80386, operation REP is interpreted as \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ |
| A | Repeat while ECX not xero |
| B | Repeat unconditionally |
| C | Repeat while ECX xero |
| D | None of these |
| Answer | A |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | NOP occupies a byte of storage but affects nothing but \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_. |
| A | The stack pointer. |
| B | The program counter. |
| C | The instruction pointer. |
| D | None of these |
| Answer | C |
| Marks | 1 |
| Unit | 2 |

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|  |  |
| --- | --- |
| Id |  |
| Question | The operations specified by the instruction are executed during \_\_\_\_\_\_\_\_\_\_\_\_\_ |
| A | execute step |
| B | fetch step |
| C | decode step |
| D | Operand fetch step |
| Answer | A |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | A new instruction is read from the external memory during\_\_\_\_\_\_\_\_\_\_\_\_\_ |
| A | fetch step |
| B | execute step |
| C | output cycle time |
| D | input step |
| Answer | A |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | The parallel instruction execution is preferred because \_\_\_\_\_\_\_\_\_\_\_ |
| A | It requires less memory |
| B | Circuitry is simple |
| C | It is faster than serial operation |
| D | All of these |
| Answer | C |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | SUB means |
| A | Subtract from Accumulator Using borrow |
| B | Subtract Immediate from Accumulator Using Borrow Flag |
| C | Subtract Immediate data from Accumulator |
| D | Subtract from Accumulator |
| Answer | D |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | Zero address instruction format is used for |
| A | RISC architecture. |
| B | CISC architecture. |
| C | Von-Neuman architecture. |
| D | Stack-organized architecture |
| Answer | D |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | CPU executes the instruction in their stored sequence except when the execution sequence is explicitly altered by a \_\_\_\_\_\_\_\_\_\_\_ |
| A | branch instruction |
| B | ADD instruction |
| C | SUB instruction |
| D | MULT instruction |
| Answer | A |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | The overlapping of instruction fetching and execution is an example of \_\_\_\_\_\_\_\_\_\_\_\_\_ |
| A | Fetch step |
| B | Execute step |
| C | instruction pipe lining |
| D | Instruction execution |
| Answer | C |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | An instruction D2:=D2+M(ADR1)combines\_\_\_\_\_\_\_\_\_\_ operations. |
| A | Store and add |
| B | Store and load |
| C | load and add |
| D | None of above |
| Answer | C |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | RISC tend to have\_\_\_\_\_\_\_\_ instruction format. |
| A | few |
| B | large |
| C | 64 bit |
| D | More opcode |
| Answer | A |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | The\_\_\_\_\_\_\_\_\_\_\_\_ family is a microprocessor series with many different instruction formats and sizes and supports more operand addressing modes. |
| A | ARM 6 |
| B | None of these |
| C | MIPS |
| D | Motorola 680X0 |
| Answer | D |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | The purpose of an instruction is to specify both an operation and \_\_\_\_\_\_\_\_\_\_\_\_\_ |
| A | Set of operands |
| B | Set of registers |
| C | Set of memory locations |
| D | Set of instruction |
| Answer | A |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | In an instruction, an operation is specified by a field called\_\_\_\_\_\_ |
| A | addresses |
| B | op-code |
| C | operands |
| D | operation |
| Answer | B |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | The explicit address fields refer to\_\_\_\_\_\_\_\_\_ registers or memory locations while implicit addresses refers to \_\_\_\_\_\_ registers. |
| A | special purpose & general purpose CPU |
| B | general purpose CPU & special purpose |
| C | Data registers & address registers |
| D | address registers & Data registers |
| Answer | B |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | Load instruction belongs to\_\_\_\_\_ group of instructions. |
| A | Data transfer |
| B | Data processing |
| C | Program control |
| D | None of these |
| Answer | A |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | Branch instruction belongs to\_\_\_\_\_ group of instructions. |
| A | Data transfer |
| B | Data processing |
| C | Program control |
| D | None of these |
| Answer | C |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | A \_\_\_\_ is used to indicate computation status or exceptional conditions resulting from the execution of instruction. |
| A | Status register |
| B | data register |
| C | program counter |
| D | none of these |
| Answer | A |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | Which of the following typically involves instructions of fixed length? |
| A | CISC |
| B | RISC |
| C | Intel 8086 |
| D | None of these |
| Answer | B |
| Marks | 1 |
| Unit | 2 |
| Id |  |
| Question | Large no. of instructions and types lead to |
| A | Simple control unit |
| B | Complex control unit |
| C | Medium level complex control unit |
| D | None of these |
| Answer | B |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | Maximum instruction length of Motorola 680X0 is |
| A | 10 bytes |
| B | 12 bytes |
| C | 16 bytes |
| D | 8 bytes |
| Answer | A |
| Marks | 1 |
| Unit | 2 |

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|  |  |
| --- | --- |
| Id |  |
| Question | The world's first microprocessor, the intel 4004, was\_\_\_\_bit microprocessor |
| A | 4 |
| B | 6 |
| C | 8 |
| D | 16 |
| Answer | A |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | Which of the following statement related to 4040 microprocessor is true in comparison with 4004 microprocessor? |
| A | Enhancement in speed |
| B | Improvement in word length |
| C | Improvement in memory size |
| D | None of these |
| Answer | A |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | Which of the following are the 8 bit microprocessor? |
| A | 8008 |
| B | 8080 |
| C | 8085 |
| D | All of these |
| Answer | D |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | The 8008 came up with\_\_\_\_\_ memory size. |
| A | 1kbytes |
| B | 4kbytes |
| C | 16kbytes |
| D | 64kbytes |
| Answer | C |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | The 4004 microprocessor has\_\_\_\_\_ instructions. |
| A | 32 |
| B | 45 |
| C | 48 |
| D | 64 |
| Answer | B |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | The 8008 microprocessor has\_\_\_\_\_\_ instructions. |
| A | 32 |
| B | 45 |
| C | 48 |
| D | 64 |
| Answer | C |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | The 8080 came up with\_\_\_\_ memory size. |
| A | 1kbytes |
| B | 4kbytes |
| C | 16kbytes |
| D | 64kbytes |
| Answer | D |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | The 8085 came up with\_\_\_\_\_ memory size. |
| A | 1kbytes |
| B | 4kbytes |
| C | 16kbytes |
| D | 64kbytes |
| Answer | D |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | \_\_\_\_\_\_was the first Intel family member designed specifically for use as a CPU in a multi-user microcomputer. |
| A | 8086 |
| B | 80186 |
| C | 80286 |
| D | 80386 |
| Answer | C |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | The 8086 is a\_\_\_\_\_\_ microprocessor. |
| A | 8-bit |
| B | 16-bit |
| C | 32-bit |
| D | 24-bit |
| Answer | B |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | The Execution Unit of 8086 consists of\_\_\_\_ |
| A | ALU |
| B | flag register |
| C | pointer and index registers |
| D | all of these |
| Answer | D |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | The Arithmetic Logic Unit of 8086 is of \_\_\_\_ bits. |
| A | 8 |
| B | 16 |
| C | 20 |
| D | 24 |
| Answer | B |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | The actions of CPU during instruction cycle are defined by a sequence of micro operations, each of which typically involves \_\_\_\_\_\_ |
| A | Memory transfer operation |
| B | Register transfer operation |
| C | Gate level operation |
| D | None of these |
| Answer | B |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | IAS computer stands for\_\_\_\_ |
| A | Institute for Advanced Systems |
| B | Institute for Advanced Services |
| C | Institute for Advanced Studies |
| D | None of these |
| Answer | C |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | LOAD / STORE Architecture is \_\_\_\_\_ |
| A | CISC Architecture |
| B | RISC Architecture |
| C | Stack Architecture |
| D | None of these |
| Answer | B |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | Identify fthe exception out of the following statements |
| A | Maskable Interrupt |
| B | Divide by Zero Interrupt |
| C | Non maskable Interrupt |
| D | None of these |
| Answer | B |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | In CPU Motorola 680X0, half word data representation means |
| A | 16 bits |
| B | 8 bits |
| C | 32 bits |
| D | 4 bits |
| Answer | A |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | In the event of an interrupt, the CPU performs which action? |
| A | Halts execution of currently executing program. |
| B | Suspends execution of currently executing program. |
| C | Do not halt currently executing program. |
| D | None of these. |
| Answer | B |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | I /O ports are \_\_\_\_\_\_\_\_ |
| A | I/O buses |
| B | Addressable Registers |
| C | Addressable memory |
| D | None of these |
| Answer | B |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | Processors of all computers, whether micro, mini or mainframe must have |
| A | ALU |
| B | Primary Storage |
| C | Control unit |
| D | All of above |
| Answer | All of above |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | CPU does not perform the operation \_\_\_\_\_\_\_\_\_\_ |
| A | data transfer |
| B | logic operation |
| C | arithmetic operation |
| D | all of the above |
| Answer | data transfer |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | A simple way of performing I/O tasks is to use a method known as ...................... |
| A | program-controlled input |
| B | program-controlled output |
| C | I/O operation |
| D | program-controlled I/O |
| Answer | D |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | An exception conditions in a computer system by an event external to the CPU is called ......... |
| A | Interrupt |
| B | halt |
| C | wait |
| D | process |
| Answer | A |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | When the CPU detects an interrupt, it then saves its ................... |
| A | Current state |
| B | Previous state |
| C | Next state |
| D | Both A and B |
| Answer | A |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | SIMD stands for .... |
| A | Single Instruction Stream Over Main Data Stream |
| B | Single Instruction Stream Over Minimum Data Streams |
| C | Single Instruction Stream Over Single Data Stream |
| D | Single Instruction Stream Over Multiple Data Streams |
| Answer | D |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | MIMD stands for \_\_\_\_\_ |
| A | Multiple instruction multiple data |
| B | Multiple instruction memory data |
| C | Memory instruction multiple data |
| D | Multiple information memory data |
| Answer | A |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | Which of the following architecture is/are not  suitable for realizing SIMD |
| A | Vector Processor |
| B | Array Processor |
| C | Von-Neumann |
| D | All of the above |
| Answer | C |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | For each instructions of program in memory the CPU goes through a |
| A | decode - fetch - execute sequence |
| B | execute - store - decode sequence |
| C | fetch - decode - execute sequence |
| D | fetch - execute - decode sequence |
| Answer | C |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | Which of the following is the fastest |
| A | CPU |
| B | magnetic tapes and disks |
| C | video terminal |
| D | sensors, mechanical controllers |
| Answer | A |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| **Id** |  |
| Question | Processors of all computers, whether micro, mini or mainframe must have\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ |
| A | ALU |
| B | Primary Storage |
| C | Control unit |
| D | All of above |
| Answer | D |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| **Id** |  |
| Question | CPU does not perform the operation \_\_\_\_\_\_\_\_\_\_ |
| A | data transfer |
| B | logic operation |
| C | arithmetic operation |
| D | all of the above |
| Answer | A |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| **Id** |  |
| Question | A simple way of performing I/O tasks is to use a method known as \_\_\_\_\_\_\_\_\_\_\_\_ |
| A | program-controlled input |
| B | program-controlled output |
| C | I/O operation |
| D | program-controlled I/O |
| Answer | D |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| **Id** |  |
| Question | When the CPU detects an interrupt, it then saves its \_\_\_\_\_\_\_\_\_\_ |
| A | Current state |
| B | Previous state |
| C | Next state |
| D | Both A and B |
| Answer | A |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| **Id** |  |
| Question | In an accumulator based CPU M(adr):=AC means |
| A | Transfer a word from accumulator to memory |
| B | Transfer a word from memory to accumulator |
| C | Transfer a word from address to accumulator |
| D | Transfer a word from memory address to memory |
| Answer | A |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| **Id** |  |
| Question | In an accumulator based CPU AC :=M(adr) means |
| A | Transfer a word from accumulator to memory |
| B | Transfer a word from memory to accumulator |
| C | Transfer a word from address to accumulator |
| D | Transfer a word from memory address to memory |
| Answer | B |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| **Id** |  |
| Question | In an accumulator based CPU, DR:=AC means |
| A | Move contents of accumulator to DR |
| B | Transfer a word from DR to accumulator |
| C | Transfer a word from address to accumulator |
| D | Transfer a word from memory address to DR |
| Answer | A |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| **Id** |  |
| Question | For each instructions of program in memory the CPU goes through a |
| A | decode - fetch - execute sequence |
| B | execute - store - decode sequence |
| C | fetch - decode - execute sequence |
| D | fetch - execute - decode sequence |
| Answer | C |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| **Id** |  |
| Question | The maximum addressing capacity of a micro processor which uses 16 bit database & 32 bit address base is |
| A | 64K |
| B | 4GB |
| C | Both A & B |
| D | None of these |
| Answer | B |
| Marks | 1 |
| Unit | 2 |

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Course

|  |  |
| --- | --- |
| Id |  |
| Question | Which of the following registers is used to keep track of address of the memory location where the next instruction is located? |
| A | Instruction Register |
| B | Memory Address Register |
| C | Memory Data Register |
| D | Program Counter |
| Answer | D |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | The program counter Is \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ |
| A | a accumulator |
| B | a register |
| C | a counter |
| D | used to store the operands |
| Answer | B |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | The register which contains the data to be written into or read out of the addressed location is known as |
| A | index register |
| B | memory address register |
| C | memory data register |
| D | program counter |
| Answer | C |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | The content of a 4-bit register is initially 1101. The register is shifted 2 times to the right with the serial input being 1011101.  What is the content of the register after each shift? |
| A | 1110, 0111 |
| B | 0001, 1000 |
| C | 1101, 1011 |
| D | 1001, 1001 |
| Answer | A |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | The register which keeps track of the execution of a program and which contains the memory address of the next instruction to be executed is known as |
| A | Instruction Register |
| B | Memory Address Register |
| C | Memory Data Register |
| D | Program counter |
| Answer | D |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | Which of the following is used as storage locations both in the ALU and in the control section of a computer |
| A | accumulator |
| B | register |
| C | adder |
| D | decoder |
| Answer | B |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | Accumulator is a |
| A | hardwired unit |
| B | sequential circuit |
| C | finite state machine |
| D | register |
| Answer | D |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | A register organized to allow to move left or right operations is called |
| A | Counter |
| B | Loader |
| C | Shift register |
| D | adder |
| Answer | C |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | A register capable of shifting its binary information either to the right or the left is called a |
| A | parallel register |
| B | serial register |
| C | shift register |
| D | storage register |
| Answer | C |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | What is the content of Stack Pointer (SP)? |
| A | Address of the current instruction |
| B | Address of the next instruction |
| C | Address of the top element of the stack |
| D | Size of the stack. |
| Answer | C |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | The operation executed on data stored in registers is called |
| A | Macro-operation |
| B | Micro-operation |
| C | Bit-operation |
| D | Byte-operation |
| Answer | B |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | Status bit register is called \_\_\_\_\_\_\_\_register |
| A | binary |
| B | flag |
| C | signed |
| D | unsigned |
| Answer | B |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | What is the content of Stack Pointer (SP)? |
| A | Address of the current instruction |
| B | Address of the next instruction |
| C | Address of the top element of the stack |
| D | Size of the stack. |
| Answer | C |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | The operating mode(s) of 8086 is/are\_\_\_\_\_\_. |
| A | minimum mode |
| B | maximum mode |
| C | protected mode |
| D | a and b |
| Answer | D |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | The 8086 has \_\_\_\_\_\_ data bus. |
| A | 8-bit |
| B | 16-bit |
| C | 24-bit |
| D | 32-bit |
| Answer | B |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | The 8086 can access up to\_\_\_\_\_\_ locations. |
| A | 64kbytes |
| B | 1Mbytes |
| C | 16Mbytes |
| D | 64Mbytes |
| Answer | B |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | The 8086 has\_\_\_\_\_\_ address bus. |
| A | 8-bit |
| B | 16-bit |
| C | 20-bit |
| D | 24-bit |
| Answer | C |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | The 8086 can access up to\_\_\_\_\_\_ I/O ports. |
| A | 256 |
| B | 1024 |
| C | 65536 |
| D | 1 Mbytes |
| Answer | C |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | The instruction of 8086 is\_\_\_\_\_\_ bytes |
| A | 2 |
| B | 4 |
| C | 6 |
| D | 8 |
| Answer | C |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | For 8086,\_\_\_\_\_\_\_ bus is bi-directional and \_\_\_\_\_\_\_\_ bus is unidirectional. |
| A | address, data |
| B | data, address |
| C | control, data |
| D | address, control |
| Answer | B |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | Which of following is/are the function(s) of BIU ? |
| A | To send address of memory/IO |
| B | To fetch instruction from memory |
| C | To support instruction queuing |
| D | All of these |
| Answer | D |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | The BIU of 8086 consists of\_\_ |
| A | segment registers |
| B | instruction queue |
| C | instruction pointer |
| D | All of these |
| Answer | D |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | The segment register of 8086 is \_\_\_ bit. |
| A | 8 |
| B | 16 |
| C | 20 |
| D | 24 |
| Answer | B |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | The instruction pointer of 8086 is \_\_\_\_\_ bit. |
| A | 8 |
| B | 16 |
| C | 20 |
| D | 24 |
| Answer | B |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | The queue of 8086 operates on principle\_\_ |
| A | LIFO |
| B | FIFO |
| C | LILO |
| D | FILO |
| Answer | B |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | Feature of fetching the next instruction while the current instruction is executing is called\_\_ |
| A | Fetching |
| B | Execution |
| C | Pipelining |
| D | Decoding |
| Answer | C |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | A register set of 8086 consists of\_\_\_\_ |
| A | General purpose registers |
| B | pointer registers |
| C | index registers |
| D | all of these |
| Answer | D |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | In 8086 X letter with register is used to specify\_\_\_\_ bit register. |
| A | 8 |
| B | 10 |
| C | 16 |
| D | 20 |
| Answer | C |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | The flag register of 8086 is \_ bits. |
| A | 8 |
| B | 16 |
| C | 20 |
| D | 24 |
| Answer | B |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | Each segment in the 8086 is of\_\_\_\_\_ bytes |
| A | 4kbytes |
| B | 16kbytes |
| C | 64kbytes |
| D | 1mbytes |
| Answer | C |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | During physical address calculations the segment register contents are shifted by\_\_ |
| A | 2-bits left |
| B | 4-bits right |
| C | 2-bits right |
| D | 4-bits right |
| Answer | B |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | During instruction fetch \_\_\_\_\_\_\_ and \_\_\_\_\_ registers are used. |
| A | IP,DS |
| B | CS,IP |
| C | SS,BP |
| D | SS,IP |
| Answer | B |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | \_\_\_\_ flag of 8086 is used for single stepping through a program |
| A | ZF |
| B | SF |
| C | TF |
| D | IF |
| Answer | C |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | \_\_\_\_\_\_\_ flag of 8086 is used for BCD operations |
| A | ZF |
| B | TF |
| C | IF |
| D | AF |
| Answer | D |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | Which of the Following flag status is wrong after addition of (65D1)16 and (2359)16 ? |
| A | SF=1 |
| B | PF=1 |
| C | CF=1 |
| D | AF=0 |
| Answer | C |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | Which of the following flag status is wrong after subtraction (354A)16 from (6729)16? |
| A | SF=0 |
| B | ZF=0 |
| C | PF=0 |
| D | AF=0 |
| Answer | C |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | Which of the Following flag status is/are Correct after addition of (65D1)16 and (2359)16? |
| A | SF=1 |
| B | ZF=0 |
| C | OF=1 |
| D | ALL OF THESE |
| Answer | D |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | Which of the Following flag status is/are Correct after subtraction of (354A)16 from (6729)16? |
| A | PF=1 |
| B | CF=0 |
| C | OF=0 |
| D | All of these |
| Answer | D |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | What is the minimum size of segment in 8086? |
| A | 16 bytes |
| B | 256 bytes |
| C | 1 kbytes |
| D | 64 kbytes |
| Answer | A |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | Which of the following statement is/are true ? |
| A | Segments can overlap |
| B | Segments maximum size is 64 kbytes |
| C | Segments minimum size is 16 bytes |
| D | All of these |
| Answer | D |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | ln 8086, the segment can start at any memory address which is divisible by \_\_\_\_\_\_ |
| A | 8 |
| B | 16 |
| C | 20 |
| D | 24 |
| Answer | B |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | A register organized to allow to move left or right operations is called |
| A | Counter |
| B | Loader |
| C | Shift register |
| D | adder |
| Answer | C |
| Marks | 1 |
| Unit | 2 |

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|  |  |
| --- | --- |
| Id |  |
| Question | The 80386 is a \_\_\_\_\_\_ bit microprocessor. |
| A | 16 |
| B | 20 |
| C | 32 |
| D | 64 |
| Answer | C |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | The ALU of 80386 \_\_\_\_bit. |
| A | 16 |
| B | 20 |
| C | 32 |
| D | 64 |
| Answer | C |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | The address bus of 80386DX is …. Bit. |
| A | 16 |
| B | 20 |
| C | 32 |
| D | 64 |
| Answer | C |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | The 80386DX can address up to \_\_\_\_\_ physical memory. |
| A | 1 Mbytes |
| B | 16 Mbytes |
| C | 1 Gbytes |
| D | 4 Gbytes |
| Answer | D |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | The 80386DX can address up to …… virtual memory. |
| A | 1 Terabytes |
| B | 8 TeraBytes |
| C | 16 TeraBytes |
| D | 64 TeraBytes |
| Answer | D |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | …… architecture of 80386 allows simultaneous instruction fetching, decoding and execution of instruction. |
| A | Pipelined |
| B | Harvard |
| C | Princeton |
| D | Von Neumann |
| Answer | A |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | Which of following circuitry is provided by 80386? |
| A | Virtual memory management circuitry |
| B | Protection circuitry |
| C | Multiply / Divide circuitry |
| D | All of these |
| Answer | D |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | Which of the following function units are supported by 80386 ? |
| A | Central processing unit |
| B | Memory management unit |
| C | Bus control unit |
| D | All of these |
| Answer | D |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | The execution unit of 80386 consists of ……….. |
| A | Control unit |
| B | Data Unit |
| C | Protection Test Unit |
| D | All Of These |
| Answer | D |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | Page size in 80386 is \_\_\_\_\_\_\_ |
| A | 1kbytes |
| B | 2kbytes |
| C | 4kbytes |
| D | 8kbytes |
| Answer | C |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | In 80386, which of the following signal is used to identify machine cycle? |
| A | M/IO |
| B | D/C |
| C | W/R |
| D | All of these |
| Answer | D |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | Byte enable signals provided by 80386 are used to select \_\_\_\_\_ |
| A | address bus |
| B | Data bus |
| C | Control bus |
| D | All of these |
| Answer | B |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | The data bus of 80386DX consists of\_\_\_\_\_ pins |
| A | 16 |
| B | 32 |
| C | 64 |
| D | 128 |
| Answer | B |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | The 80386DX generates \_\_\_\_\_ address. |
| A | 16-bits |
| B | 24-bits |
| C | 32-bits |
| D | 64-bits |
| Answer | C |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | The 80386DX supports \_\_\_\_\_\_simultaneously accessible memory blocks. |
| A | 4 |
| B | 6 |
| C | 8 |
| D | 16 |
| Answer | B |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | When PE = 1, 80386 operates in \_\_\_\_ mode. |
| A | Real |
| B | Virtual 8086 |
| C | Protected |
| D | All of these |
| Answer | C |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | After every task switch, 80386 sets \_\_\_\_bit. |
| A | T |
| B | TF |
| c | TS |
| d | none of these |
| Answer | C |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | Intel i7 processor supports lntel \_\_\_ architecture. |
| A | 16 |
| B | 32 |
| C | 64 |
| D | 128 |
| Answer | C |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | General purpose registers of i7 Microprocessors are \_\_\_bit. |
| A | 16 |
| B | 32 |
| C | 64 |
| D | 128 |
| Answer | C |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | Intel i7 processor has \_\_\_ general Purpose registers. |
| A | 8 |
| B | 16 |
| C | 32 |
| D | None of these |
| Answer | B |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | Intel i7 processor has \_\_\_\_bit segment registers. |
| A | 8 |
| B | 16 |
| C | 32 |
| D | None of these |
| Answer | B |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | Intel i7 processor has \_\_\_segment registers. |
| A | 6 |
| B | 8 |
| C | 12 |
| D | 16 |
| Answer | A |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | Intel i7 processor has \_\_\_ bit RFLAG register. |
| A | 8 |
| B | 16 |
| C | 32 |
| D | 64 |
| Answer | D |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | Intel i7 processor has \_\_\_\_bit RIP register. |
| A | 8 |
| B | 16 |
| C | 32 |
| D | 64 |
| Answer | D |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | Intel i7 processor has \_\_\_bit floating point data registers. |
| A | 24 |
| B | 32 |
| C | 64 |
| D | 80 |
| Answer | D |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | Which of the following is/are the FPU Registers of lintel i7 processor? |
| A | Control register |
| B | Status register |
| C | Tag register |
| D | All of these |
| Answer | D |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | The size of an opcode register of i7 processor is \_\_\_\_bit. |
| A | 8 |
| B | 11 |
| C | 16 |
| D | 32 |
| Answer | B |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | Intel i7 Processor has \_\_\_\_floating point data registers. |
| A | 8 |
| B | 12 |
| C | 16 |
| D | 24 |
| Answer | A |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | Which of the following registers is not the part of i7 processor ? |
| A | FPU registers |
| B | MMX registers |
| C | XMM registers |
| D | None of these |
| Answer | D |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | Intel i7 processor has \_\_\_\_\_\_MMX registers. |
| A | 8 |
| B | 16 |
| C | 32 |
| D | 64 |
| Answer | A |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | Intel i7 processor has \_\_\_\_\_XMM registers |
| A | 8 |
| B | 16 |
| C | 32 |
| D | 64 |
| Answer | B |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| Id |  |
| Question | With the help of \_\_\_\_\_\_\_\_control bit 80386 sets detects whether 80287 or 80387 is connected in the system |
| A | EM |
| B | ET |
| C | MP |
| D | None of these |
| Answer | B |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| **Id** |  |
| Question | Intel®\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ Technology of i7 microprocessor reduces idle power via power gates, and automated low-power states. |
| A | Hyper-Threading |
| B | Intelligent Power |
| C | Turbo Boost |
| D | vPro™ |
| Answer | B |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| **Id** |  |
| Question | Intel® \_\_\_\_\_\_\_\_\_\_Technology of i7 microprocessor does concurrent multi-threading and boosts performance in parallel applications. |
| A | Intelligent Power |
| B | Turbo Boost |
| C | vPro™ |
| D | Hyper-Threading |
| Answer | D |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| **Id** |  |
| Question | Intel® \_\_\_\_\_\_\_\_\_ technology of i7 microprocessor has features remote management, flexible virtualization, and enhanced security capabilities. |
| A | Hyper-Threading |
| B | vPro™ |
| C | Intelligent Power |
| D | Turbo Boost |
| Answer | B |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| **Id** |  |
| Question | Intel®\_\_\_\_\_\_\_\_\_\_\_\_\_ Technology of i7 microprocessor boosts performance by increasing processor frequency. |
| A | vPro™ |
| B | Hyper-Threading |
| C | Turbo Boost |
| D | Intelligent Power |
| Answer | C |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| **Id** |  |
| Question | Intel 80386Dx uses very large address space as\_\_\_\_\_\_\_\_\_\_\_ of physical address space. |
| A | 8 gigabyte |
| B | 16 gigabyte |
| C | 32 gigabyte |
| D | 4 gigabyte |
| Answer | D |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| **Id** |  |
| Question | Virtual mode flag bit can be set using \_\_\_\_\_\_\_ instruction. |
| A | IRET |
| B | IERT |
| C | POPF |
| D | NOP |
| Answer | A |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| **Id** |  |
| Question | The 32-bit\_\_\_\_\_\_\_\_\_\_\_\_model of the 386 is the most important feature change in memory for the x86 processor family . |
| A | threshold |
| B | normalized |
| C | flat memory |
| D | binary |
| Answer | C |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| **Id** |  |
| Question | The 80386 featured three operating modes: real mode, \_\_\_\_\_\_\_\_mode and virtual mode. |
| A | normal |
| B | protected |
| C | Non real |
| D | None of these |
| Answer | B |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| **Id** |  |
| Question | The two chip platform of\_\_\_\_\_\_\_\_\_\_\_\_ consists of a processor and platform controller hub and enables higher performance and easier validation. |
| A | Motorola 68020 |
| B | i7 microprocessor |
| C | 80386Dx |
| D | Arm6 |
| Answer | B |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| **Id** |  |
| Question | Intel core i7 desktop processor series are the next generation of\_\_\_ bit multi-core processors built on 45 -nanometer process technology. |
| A | 128 |
| B | 64 |
| C | 32 |
| D | 256 |
| Answer | B |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| **Id** |  |
| Question | \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ is two-chip platform processors with integrated dual-channel DDR3 memory controller and flexible x16 PCI Express\* 2.0 controller resulting in board real estate. |
| A | Intel core i7 |
| B | 80386Dx |
| C | Arm6 |
| D | Motorola 68020 |
| Answer | A |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| **Id** |  |
| Question | Intel 80386Dx uses \_\_\_\_\_\_\_\_\_\_\_of maximum segment size. |
| A | 8 gigabyte |
| B | 16 gigabyte |
| C | 32 gigabyte |
| D | 4 gigabyte |
| Answer | D |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| **Id** |  |
| Question | Intel 80386Dx uses \_\_\_\_\_\_\_\_\_\_\_of maximum segment size. |
| A | 8 gigabyte |
| B | 16 gigabyte |
| C | 32 gigabyte |
| D | 4 gigabyte |
| Answer | D |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| **Id** |  |
| Question | Intel 80386Dx uses very large address space as\_\_\_\_\_\_\_\_\_\_\_ of virtual address space. |
| A | 128 terabyte |
| B | 64 terabyte |
| C | 16 terabyte |
| D | 32 terabyte |
| Answer | B |
| Marks | 1 |
| Unit | 2 |

|  |  |
| --- | --- |
| **Id** |  |
| Question | After reset 80386 starts from memory location \_\_\_\_\_\_\_\_\_\_ under the \_\_\_\_\_\_\_\_\_\_ address mode |
| A | FFFFFFFAH, Virtual86 |
| B | FFFFFFF0H, Protected |
| C | FFFFFF80H, Real |
| D | FFFFFFF0H, Real |
| Answer | D |
| Marks | 1 |
| Unit | 2 |